Title:
The Estimation Method of Intrabay Pattern in Semiconductor Process using Simulation

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Introduction:
Recently, the semiconductor market is growing rapidly and new semiconductor factories are being built both domestically and overseas. Semiconductor factories will determine the layout of equipment and logistics equipment through various simulations. Equipment and logistics equipment used in semiconductor processing are more expensive than other equipment. So determining the initial layout is important because it costs a lot of money to move the installed equipment once. Therefore, it is not possible to construct a new layout of the existing semiconductor factory because of expensive facility moving cost. On the other hand, it is possible to change the layout of relatively inexpensive logistics equipment. In the semiconductor logistics system OHT(Overhead Hoist Transport) is used to move the target product, and the OHT moves along the rail on the ceiling.

Semiconductor logistics process efficiency is determined by various factor such as rail pattern, dispatching rule, and number of OHTs. In the semiconductor process, OHT has a effect on the efficiency of the logistics, and there are many previous related studies. One of the research areas is research on the cause of deadlock and the solution of deadlock while OHT moves [2], [7], [11]. Also, the dispatching rule that determines the route of the OHT is under study in the semiconductor process logistics [3], [4], [5], [10]. There are other studies on AMHS systems [1], [6], [8], [9]. Although there are various studies on the semiconductor process logistics, there are not many studies on intrabay pattern. Deadlock can occur depending on the intrabay pattern and even if the OHT is controlled by a good dispatching rule, good performance cannot be achieved unless it is supported by intrabay pattern. In this paper, we propose an estimation method to select the intrabay pattern of the semiconductor process and present a limit.

Main Idea:
At present, intrabay pattern in semiconductor process is determined by designer's experience and knowhow. However, there is no criterion to estimate whether the intrabay pattern thus determined is an optimal pattern. Therefore, it is necessary to select patterns by statistical methods through various experiments in various situations. As an experimental method, we model the semiconductor plant containing the target intrabay and select the number of OHTs as shown in Fig. 1 Fig. 1 is a layout that is simply modified for this paper because it minimizes the actual semiconductor factory. In the Fig. 1, the garget intrabay is indicated by a dotted line. In this paper, 3-lane intrabay is performed. The process has 77 facilities and 40 OHTs. The selection of OHT algebra will be explained later. Many scenarios and various patterns are required to select the optimal intrabay pattern for the target semiconductor factory.

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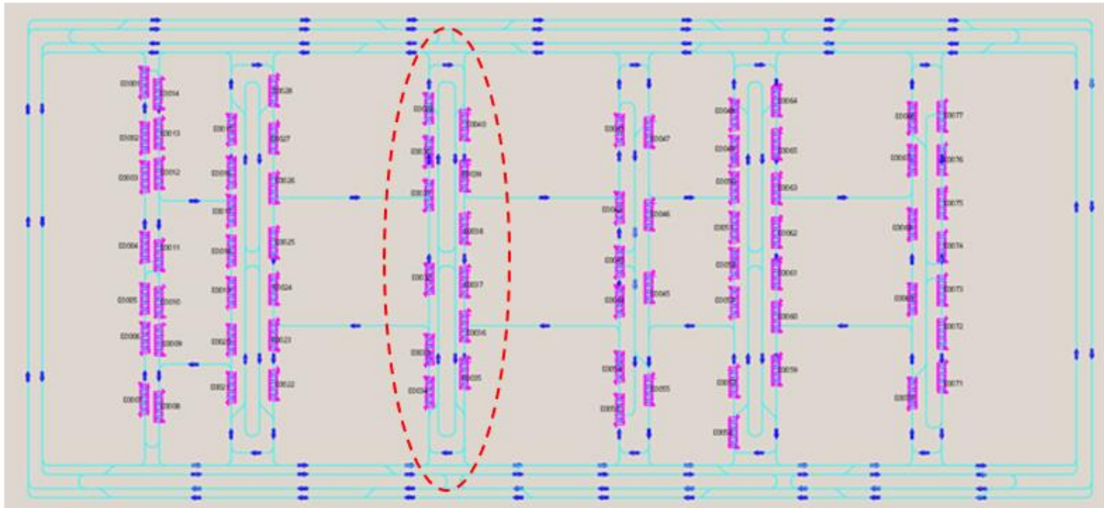

Fig. 1: Semiconductor process layout.

First, to create a scenario, from-to information between each facility is used for the target semiconductor process data. There is interval time from-to so that the amount of flow between facilities is regularly generated. Each interval time represents the amount of volume, and the shorter the interval time, the greater the amount of volume. The total from-to data is 1335, and the data is adjusted to be 1000 requests in one hour. This semiconductor factory required 40 OHTs, because it can handle 25 requests per hour. The data was generated randomly using excel, and the variance was made not to exceed 0.5. The flow amount thus created becomes one process scenario. In this paper, the flow amount is set to 100, because it requires a lot of experimental data in various situations. As shown in Fig. 2 In order to express the concentration situation, data is randomly generated by dividing the flow amount into 20(top, bottom, left, right, general). In order to concentrate the volume of the facility, increase the flow amount of the from-to data including the facility and reduce the flow amount of the from-to data of the non-included facility so that the total volume of the target intrabay is constant we created the data to keep it. As shown in Fig. 3, AutoMod of Applied Materials was used for the simulation of the semiconductor process. In Fig. 3, ‘x’ indicates are facilities and the color of the box shown the status of the OHT. (black: idle, orange: full, green: empty)

Second, we need a variety of patterns. In order to make the pattern of 3-lanes, it is necessary to arrange the circulating branch and the N branch in various ways. If the distance between branches is too short or the number of branches becomes large, jamming or dead lock may occur. Considering these factors, the pattern is divided into three areas of movement, insertion, and creation. As shown in Fig. 5, a total of 22 patterns were generated and 44 patterns were tested considering the symmetry pattern. As shown in Fig. 4 The pattern of the creation part is designed by the designer without any rule.

If one scenario is executed in one pattern, a performance evaluation index for the pattern should be presented. The indicators are as follows.

- Assignment Time (AT): Idle time of OHT.
- Time to Load (TL): Time the OHT goes to load.
- Time to Unload (TU): Time the OHT goes to unload.
- Delivery Time (DT): AT + TL + TU.
- Travel Time(TT): TL + TU.
- Number of Delay (ND): Number of OHTs with AT over 5 minutes per hour.
- Work Load (WL): TT rate per hour of OHT.

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The performance of the pattern is evaluated using AT, DT, TT, ND, and WL in the above index. AT, DT, TT, and ND are good patterns as the numerical value is low, and WL is closer to 80%, which is a good pattern. (WL's target value can be changed as a standard provided by a collaborating company.)

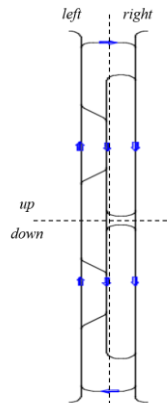

Fig. 2: Volume concentration area in the pattern.

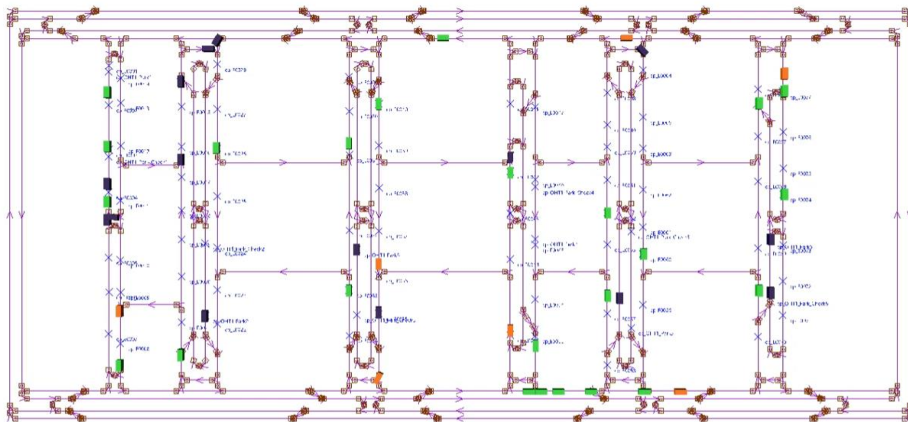

Fig. 3: Simulation of AutoMod.

Conclusions:

The experiment was performed with 4,400 simulations applying 100 scenarios for 44 patterns. For each pattern, 100 scenarios were averaged in 20 cased with 5 scenarios (top, bottom, left, right, general).

In this paper, an experiment was conducted to select optimal patterns for each situation using volume concentration situation. It is difficult to conclude that the selected pattern in this experiment will make good performance when used in other processes. The first reason is experimented in the target semiconductor process layout, so it would be different if other flow amount is applied in other process. The second reason is that the actual process simply does not move with a fixed interval time in from-to data. It is difficult to judge that the actual process has been properly simulated because it uses the simplest method for making the volume concentration situation. Third, it is hard to say that it is an optimal pattern because it artificially generates various environments and it selected using statistical methods.

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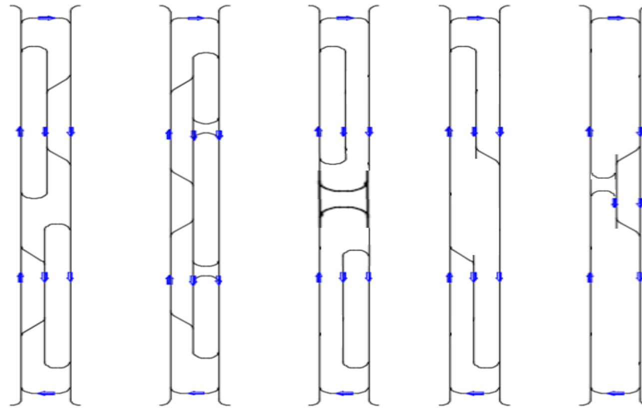
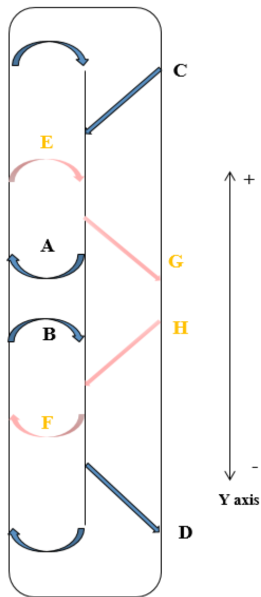


Fig. 4: Creation pattern.



	A	B	C	D	E	F	G	H
pattern1	0	0	0	0	x	x	x	x
pattern2	0	0	-6000	+6000	x	x	x	x
pattern3	+3000	-3000	0	0	x	x	x	x
pattern4	+6000	-6000	0	0	x	x	x	x
pattern5	+5000	0	0	0	x	x	x	x
pattern6	0	-5000	0	0	x	x	x	x
pattern7	0	0	-3000	0	x	x	x	x
pattern8	0	0	0	+3000	x	x	x	x
pattern9	+4000	+4000	0	0	x	x	x	x
pattern10	-4000	-4000	0	0	x	x	x	x
pattern11	0	0	0	0	insert	x	x	x
pattern12	0	0	0	0	x	insert	x	x
pattern13	0	0	0	0			insert	
pattern14	0	0	0	0				insert
pattern15	0	0	0	0	insert	insert		
pattern16	0	0	0	0			insert	insert
pattern17	0	0	0	0	insert	insert	insert	insert
pattern18	creation							
pattern19	creation							
pattern20	creation							
pattern21	creation							
pattern22	creation							

Fig. 5: Pattern generation rules.

But, since the semiconductor process is determined by the user's know-how, we believe that the proposed method will help to select better patterns. We are currently studying the experimental method proposed in this paper with the semiconductor company. In the future, we plan to study what role each pattern plays in the N-branch and the circulation branch.

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