Title:
Optimization of Nozzle Head Toolpath and Component Shape Library in Printed Electronics

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Introduction:
Additive Manufacturing (AM) based Printed Electronics (PE) is a new area where electronic components and circuits are printed directly on substrates using additive methods. The direct deposition of electrically conductive materials and associated components makes it convenient to print ultra-thin components on a variety of substrates including glass, silicon and plastic. These inherent qualities of metal powder deposition using a nozzle head makes AM based Printed Electronics a very promising manufacturing process in the area of electronic sensors and sensor networks. At present, AM based PE is a labor intensive and manual process wherein decisions are made based on the expertise and judgment of the PE designer/engineer at different stages of the process. This manual intervention at almost every step of the process increases the overall production time and also results in issues related to the consistent quality of parts. Currently, researchers are working in the area of PE for developing new materials, standards, file formats, component shapes and optimization of the nozzle head travel etc. to establish PE as the mainstream process in the electronic sensor community. Optomec [3] has developed a proprietary Aerosol Jet Process which is able to print electronic components on different planar and non-planar substrates using a layered approach. Palo Alto Research Center (PARC) has also developed a jet printing process for manufacturing organic semiconductors and conductors [2].

Earlier, the authors [5] have successfully demonstrated a neutral file format based on Constructive Solid Geometry (CSG) [6, 7] which incorporated both electric and geometric properties of the substrate and all its components. The developed file format is a hierarchical tree structure consisting of two main sub trees: geometric and electric sub-trees. It was proposed that the electric sub-tree will contain information about the electrical primitives (resistors, capacitors, diodes etc.) and will have geometric tree as its child. On the other hand, the geometric tree will store information about the geometric primitives, associated boolean operations, component material and associated tool path information. This neutral file format structure is pictorially represented in

Fig. **1**. The sample PE substrate consists of four different PE components: resistor, chip holder, diode, relay etc.

This paper will basically focus on following two areas in printed electronics:

1) Electric component shape library based on simple primitives for printed electronics.
2) Overall nozzle head travel weighted optimization to reduce build time associated with the printed electronics.

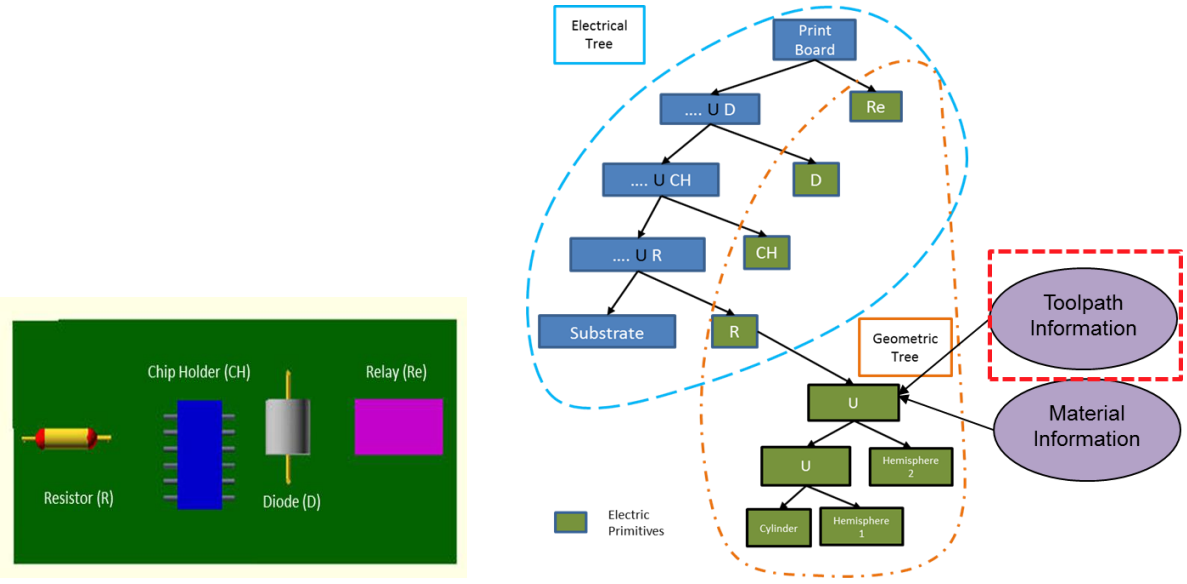


Fig. 1: Substrate with PE Components (b) A CSG based neutral file representation for PE. [5].

Main Idea:

Electric component shape library for in Printed Electronics

Apart from developing a neutral file format for PE, another important research area is to address the deficiency of a component shape library for electrical components. The idea is to select a pattern of a component from the library based on the given space constraint that will also satisfy the electrical requirement. The new pattern based on its geometry may also reduce the overall build time in printing the electrical components on the substrate using AM process. This research focuses on developing a set of new shapes for basic electric primitives such as resistors and capacitors. In PE, the electric material is deposited using a nozzle head on the substrate. This feature enables PE designer/engineer to configure different shapes of the electric primitives that will satisfy the electric functionality/property. The existing resistor and capacitors in PE are represented as shown in Fig. 2.

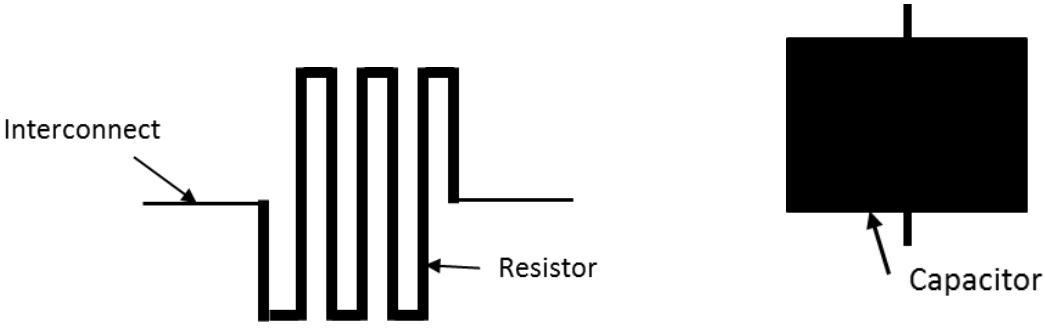
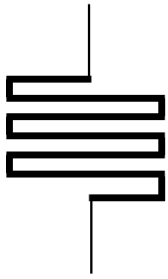
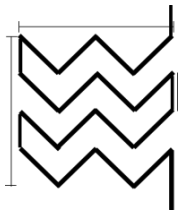


Fig. 2: (a) General representation of a resistor in PE (b) General representation of a capacitor in PE.

Preliminary results for a new resistor design within the same space constraints are presented in Tab. 1. It can be seen that using the same grid size encompassing the overall resistor design, the new shape of the resistor will have more electric current carrying conductor length as compared to the traditional resistor pattern.

Sr. No.	Pattern	Grid Size (unit*unit)	Conductor Length	Length per unit area (unit)
1.	Traditional Pattern 	0.4*0.4	2.4	15
2.	Proposed Pattern 	0.4*0.4	2.66	16.625

Tab. 1: New patterns for resistor in Printed Electronics [4].

From the proposed patterns in Tab. 1, it can be observed that each of these proposed shapes will have a unique toolpath pattern while depositing material on the substrate, which will affect the overall time required to build the components on the substrate. In addition, even the filling pattern may vary from one shape to another. This research focuses on optimizing the existing shape of the electric primitives for minimum build time and the required substrate area.

Nozzle head travel optimization during deposition:

As proposed earlier, a variety of shapes can be used in AM based PE to achieve the same required electrical property of the component. Each of these shapes may result in varied nozzle head travel based on the cross-sectional area (2D contour) of the component while depositing the material using a layer by layer approach. Previously, researchers [1] and [8] have identified critical variables such as temperature of each component, substrate area, high power component, high potential critical component etc. that may have to be considered in the placement of electrical components on a traditional printed circuit board.

A weighted optimization function that will include available space and build time as constraints is proposed and will provide the user with appropriate shapes for the electrical components and tool parameters (nozzle head diameter for printing) to facilitate the manufacturing process efficiently. Various shapes developed for electric components such as resistors and capacitors will be used to reduce the overall size of the substrate. The optimization of the nozzle head travel for depositing the material efficiently is demonstrated using a k-d tree based nearest neighbor search algorithm for printed electronics. A k-d tree is generated using the centroid information available for each of the components to find the nearest PE component for material deposition. Internally, each PE component will have its own predefined nozzle head travel path which will be followed while optimizing the overall nozzle head travel.

Fig. **3** shows the optimized nozzle head travel denoted by black lines for a substrate with a total of fourteen PE components. Once the "next nearest component" is fixed for material deposition, the nozzle head starts depositing material within the PE component from "Start Point of Deposition" and

exits the component at the “End Point of Deposition” which is predefined based on the type and shape of the PE component. The proposed toolpath optimization for PE components is shown in Fig. 3.

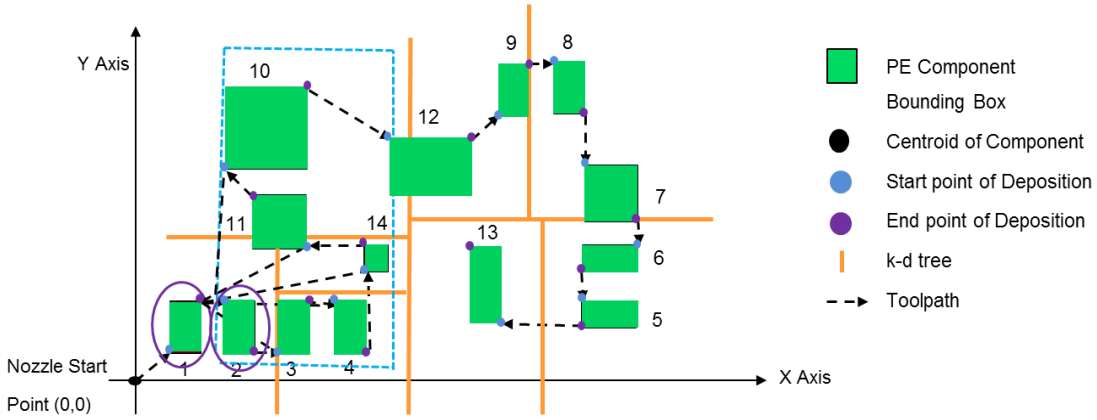


Fig. 3: Toolpath optimization for printed electronics using k-d tree based nearest neighbor search algorithm. [4].

Conclusions:

The preliminary results obtained demonstrate a need for developing new shapes/patterns for electric components in printed electronics. The associated toolpath optimization proposed for printing will reduce the overall production time and may reduce the manufacturing cost. The areas proposed in this research i.e. developing a new component shape library pertaining to printed electronics and also optimizing the nozzle head deposition toolpath to reduce the overall build time may facilitate mass production of electronic sensors and circuit boards using additive manufacturing based printed electronics.

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