Title:
3D ICs Layout Hypergraph Representation

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Introduction:
According to Moore's Law, the number of elements in a typical integrated circuit design (IC) doubles approximately every two years. The task of 3D ICs floor planning involves the assembly of millions of elements and is an enormous intellectual challenge. It relates not only to topological arrangement of components but also appropriate wiring of circuit elements to fulfill different power, timing and manufacturability requirements. No wonder that the importance of electronic design automation (EDA) tools rapidly increases.

Graphical and geometric data describing layout design is not enough to support the computer control of the design process. In order to automatically generate valid design solutions that meet requirements and fulfill constraints, the design knowledge representation is needed. Generally, either symbolic or graphical knowledge description may be applied. In the first case, facts are symbolic terms and the process of inferring involves the manipulation of these terms. In the second one, the spatial relations between components determine the structure of knowledge representation and the way it is exploit. The latter approach can be naturally adopted as a 3D ICs layout representation. This paper presents a knowledge intensive 3D ICs layout representation in the form of hypergraphs.

Main Idea:
Hypergraphs are a generalization of graphs, where not only binary but n-ary relations may be represented. In other words, the edges, called hyperedges, can connect more than two vertices. They have found many practical applications including linear algebra, information retrieval, data mining, and architectural design. Since it is straightforward to map a netlist into a hypergraph, they have also been extensively studied in ICs layout design [3]. However, the formerly proposed hypergraph representation and partitioning algorithms [1] do not take the advantage of the third dimension in the 3D space. They perform partitioning of the netlist into tiers, just like in 2D, using only single dimension and fail to give optimal solutions. The k-way partitioning assigns vertices of a hypergraph to k disjoint nonempty partitions in such a way to minimize a net cut function, which is the sum of weights of hyperedges that are cut between partitions, and to balance the total vertex weight in each partition. The optimal partitioning of a hypergraph with balance constraints is known to be NP-hard. In order to overcome the limitations, we propose to adopt the hierarchical layout hypergraphs defined in [2].

In the contrast to commonly used simple hypergraph definition with the only one type of hyperedge (a set of vertices), layout hypergraphs may have two kind of hyperedges. For the time being let us assume that they are both non-directed. The hyperedges of the first type correspond to chip components which, if necessary, may be considered at the different level of details (transistors or block-level) using a hierarchy relation. The hyperedges of the second type are used to represent relations among chip elements like adjacency or wiring. The example simple logic circuit and the corresponding layout hypergraph are presented in Fig. 1.

The proposed formalism enables to describe spatial arrangements of components including all three dimensions. With such a semantic layer chip representation the near-optimal layout solution may be found. Let us again consider the logic circuit example in Fig.1. The task is to divide the circuit in two layers so that the wire length be minimized and the number of components in each layer be balanced. The possible optimal solution is depicted in Fig. 2. The wire length treated as the distance between cells in a grid cube equals one for each pair of connected components and the number of components in both layers is perfectly balanced. Because of technological issues, any vertical connections that are not immediately adjacent may be too expensive in terms of routing resources and delay [4]. However, the cut of hyperedges between layers in such a way that all components are enclosed in the neighborhood of radius one is more preferred than minimizing a net cut function.

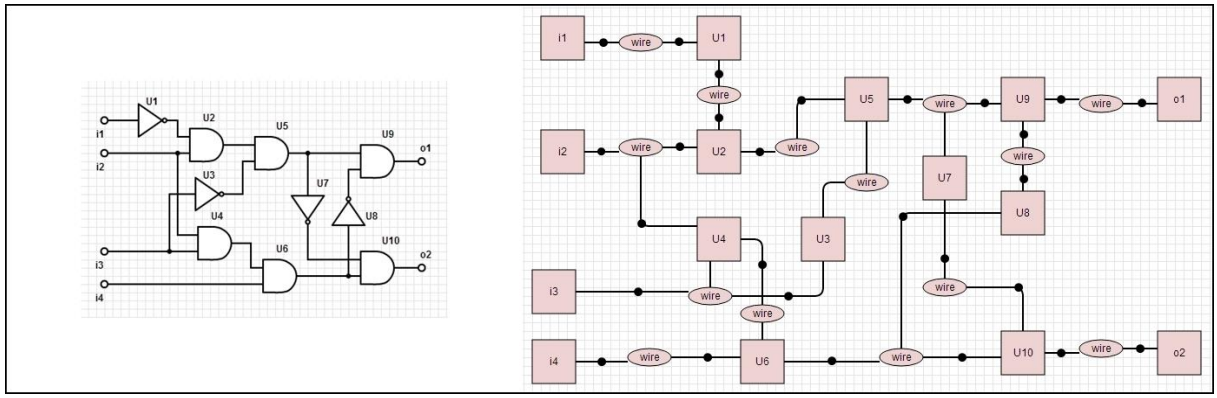

Fig. 1: The example simple logic circuit and the corresponding layout hypergraph.

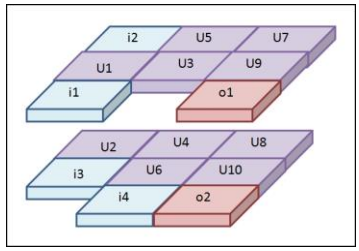

Fig. 2: The possible optimal 2-layer partitioning of the circuit in Fig. 1.

Conclusions:

The paper presents a 3D ICs layout hypergraph representation that fully reflects possible relations among chip components. Most of all, in contrast to previously proposed 3D ICs hypergraph representations, it naturally resembles spatial relations in 3D spaces. Using labeling mappings allows describing different relations among chip elements and introducing various cost functions, depending on the actual optimization task. Engaging hierarchy enables to gather and retrieve information on different levels of details. Applying hypergraph transformation rules may be used to derive important facts about the generated design solution. In the next stage of the research, the layout hypergraph representation will be applied to the task of the total wirelength minimization.

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